Abstract

The invention relates to a method for transparently maintaining cache coherency when debugging a multiple processor system with common shared memory. A software memory map representing the memory usage of the processors in the system to be debugged is created and in the software memory map is an indication of whether or not each processor has a cache. At least two debug sessions associated with two processors are activated. If an active debug session requests a write to a shared memory location, the request is executed and the software memory map is searched to located all processors having read access to that shared memory location. The write request is broadcast to each of the located processors so that each processor can perform any required cache updates.